Dual material pile gate approach for low leakage finfet

Sanjay S. Chopade, author

Abstrak

FinFET (Fin Field-Effect
Transistor) technology has recently seen a major increase in adoption
for use in integrated circuits because of its high immunity to short channel
effects and its further ability to scale
down. Previously, a major research contribution was made to reduce the leakage current in the conventional bulk devices. So many different alternatives like bulk isolation and oxide isolation are all having some pros and
cons. Here in this paper, we present a novel pile gate FinFET structure to
reduce the leakage current, as compared with Bulk FinFET without using any pstop implant or isolation oxide as in the
Silicon-on-Insulator (SOI). The major advantage of this type of
structure is that there is no need of high substrate doping, a 100% reduction in the
random dopant fluctuation (RDF) and an increase in the ION/IOFF
value. It can be very useful to improve the drain-induced barrier lowering (DIBL) at smaller technological nodes. All the work is supported by 3D TCAD simulations, using Cogenda TCAD.