Heterogeneous multicore processor technologies for embedded systems

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Deskripsi Lengkap: https://lib.ui.ac.id/detail?id=20425837&lokasi=lokal

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Abstrak

This book defines the heterogeneous multicore architecture and explains in detail several embedded processor cores including CPU cores and special-purpose processor cores that achieve highly arithmetic-level parallelism. The authors developed three multicore chips (called RP-1, RP-2, and RP-X) according to the defined architecture with the introduced processor cores. The chip implementations, software environments, and applications running on the chips are also explained in the book.

Provides readers an overview and practical discussion of heterogeneous multicore technologies from both a hardware and software point of view. Discusses a new, high-performance and energy efficient approach to designing SoCs for digitally converged, embedded systems. Covers hardware issues such as architecture and chip implementation, as well as software issues such as compilers, operating systems, and application programs. Describes three chips developed according to the defined heterogeneous multicore architecture, including chip implementations, software environments, and working applications.