

Statistical performance analysis and modeling techniques for nanometer VLSI designs

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Deskripsi Lengkap: <https://lib.ui.ac.id/detail?id=20418442&lokasi=lokal>

Abstrak

This book provides readers with tools for variation-aware design methodologies and computer-aided design (CAD) of VLSI systems, in the presence of process variations at the nanometer scale. It presents the latest developments for modeling and analysis, with a focus on statistical interconnect modeling, statistical parasitic extractions, statistical full-chip leakage and dynamic power analysis considering spatial correlations, statistical analysis and modeling for large global interconnects and analog/mixed-signal circuits.